**CPU Design Project – Part 6**

**Pavan Ravi Teja Uppu**

**Akash Tyagi**

1. **What did you learn from this project?**

We had a lot of practical skills apart from VHDL modeling, for the first time we have got a chance to test our model on a FPGA board using Altera Quartus and DE2 Board. We learnt executing a C program by developing an Instruction set and then modeling it in VHDL, It gave a closer understanding on how to implement general Algorithms by first implementing it in C and modeling it using VHDL. The course work and the project helped me understand the Hardware/ Soft-ware Interface of a Computer much better. We practically tested and verified how a computer process millions of instructions with in fraction of seconds.

1. **What would you do differently next time?**

We have Implemented a Pipeline Data path, initially our consideration was to develop a CPU with two or more Pipeline data paths with a single IF stage. So, that the Instructions can be processed parallel in a SIMD fashion. And if we still had time, we planned to plug in a Multi-Modulus Divider in a PLL for Dynamic frequency scaling by controlling the input to MMD, which was implemented as part of other course work project. But we ran out of time in the end. Next time we would like to pursue our ideas along with Hazard Detection Units in the pipelined data path.

1. **What is your advice to someone who is going to work on a similar project?**

While Implementing Pipeline Data path, we have come across time synchronization uses between the Inputs and control signals reaching the multiplexer. Result of which led to processing of different Instruction’s data which are already in the pipeline .we inspected all the multiplexers and registers in the last moment to get the errors rectified. This we feel is the most common issue in the pipeline data path. Plan your circuit carefully before writing the VHDL modules, start to work on this project ahead since you can extend the project with many modules like hazard prevention, superscalar path, etc. If an error shows up try be as specific as possible. Debug the errors instruction by instruction and in every instruction try to find out the Component at which the error occurred by inspecting the VHDL simulation of control signals and outputs of each and every component and make the necessary modifications.